What is claimed is:

1. A method for packaging a multi-chip module, comprising the steps of:

connecting a first chip having thereon wafer bumps to lower parts of inner leads of TAB tapes having the inner lead and an outer lead, thereby electrical signals being communicated therebetween;

connecting a second chip having thereon wafer bumps to an upper part of the TAB tapes connected to the first chip, thereby electrical signals being communicated therebetween; and

executing an encapsulation step, wherein an underfill material is filled in a connecting portion between the TAB tapes and the chips.

2. The method of claim 1, further comprising the steps of:

connecting a third chip having thereon wafer bumps to an upper part of the second chip;

connecting an outer lead of the TAB tape to one of the wafer bumps of the third chip;

connecting an inner lead of a TAB tape having the inner lead and an outer lead to the other wafer bump of the third chip;

connecting a fourth chip having wafer bumps to the TAB

tapes; and

executing an encapsulation step, wherein an underfill material is filled in a connecting portion between the TAB tapes and the third and forth chips.

3. The method of claim 1, further comprising the step of connecting the outer lead of the TAB tape connected to the first chip to a patterned circuit.

4. The method of claim 1, further comprising the step of mounting a radiator after a conductive adhesive is coated on an upper part of the second chip.

5. The method of claim 1, wherein the chips and the TAB tapes are connected to each other by using gang bonding or single point bonding method.

6. The method of claim 5, wherein the chips and the TAB tapes are connected to each other by bonding the inner leads of the TAB tapes to the wafer bumps of the chips.

7. The method of claim 2, further comprising the step of connecting the outer lead of the TAB tape connected to the first chip to a patterned circuit.

8. The method of claim 2, further comprising the step of

mounting a radiator after a conductive adhesive is coated on an upper part of the second chip.

9. The method of claim 2, wherein the chips and the TAB tapes are connected to each other by using gang bonding or single point bonding method.

10. The method of claim 9, wherein the chips and the TAB tapes are connected to each other by bonding the inner leads of the TAB tapes to the wafer bumps of the chips.

11. The method of claim 2, further comprising the step of accumulating a plurality of chips having thereon wafer bumps and a plurality of TAB tapes having an inner lead and an outer lead on the fourth chip.